

## Background and Highly Reliable Cells(HRCs)

**Abstract**  
 Recently, the miniaturization process has brought an increase in the failure rate of transistors. We propose new standard cells called **Highly Reliable Cells (HRCs)** to decrease the failure rate. HRCs can correct and detect transistor faults. A functional unit with HRCs achieves higher fault tolerance. The area of the unit is approximately 1.4 times larger compared to traditional cells.

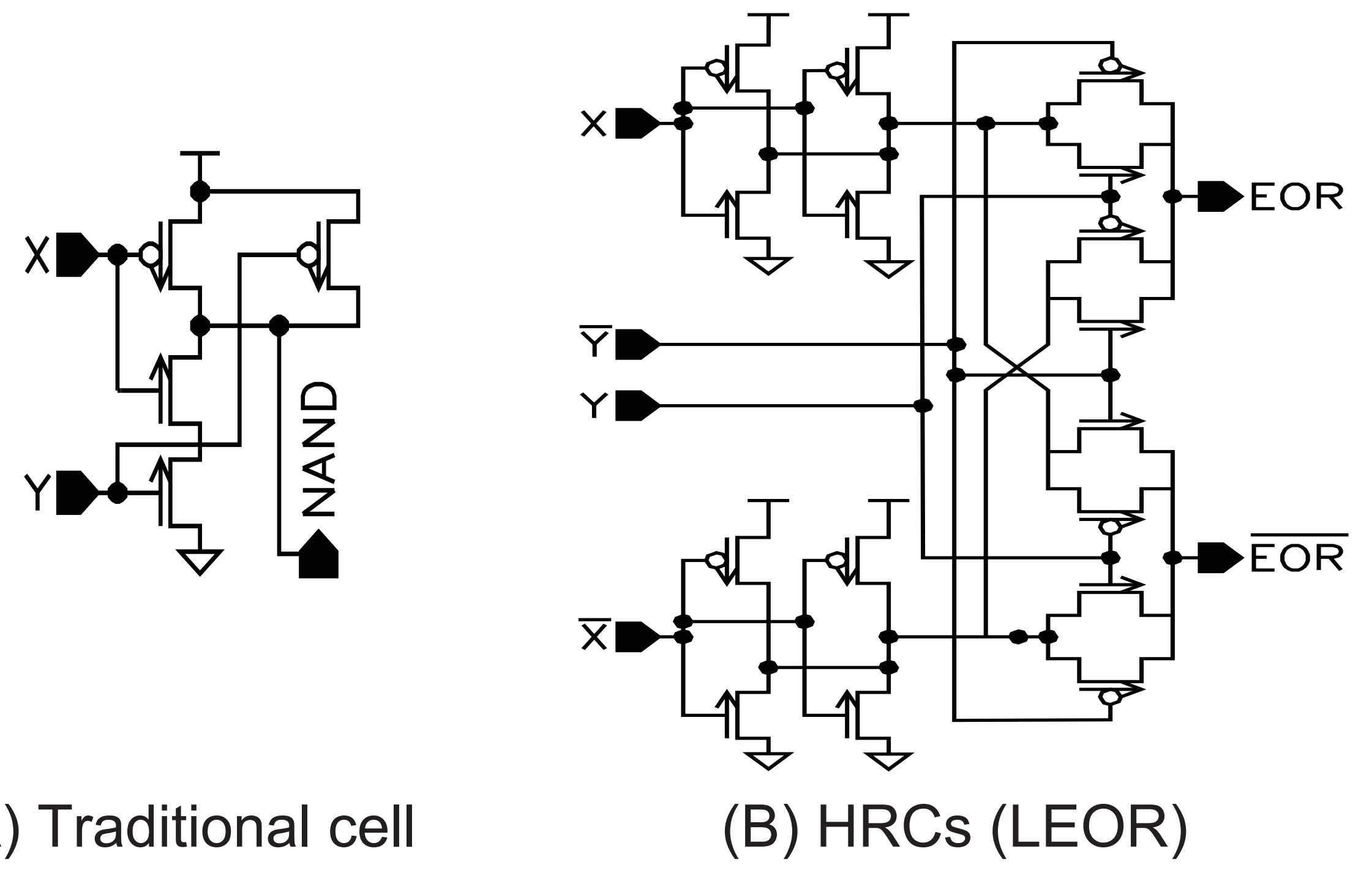
HRCs increasing rate to the total cell variety is a small, to increase the reliability of the circuit. HRCs output **the correct value** or **the wrong value**. The wrong value will indicate that the circuit had faults and the result is not valid.

- Three features of HRCs;
  - (A) An HRC will work correctly even if one transistor has a fault
  - (B) If more than two transistors have faults, an HRC will output the wrong value
  - (C) If the input contains the wrong value, the output will be the wrong value



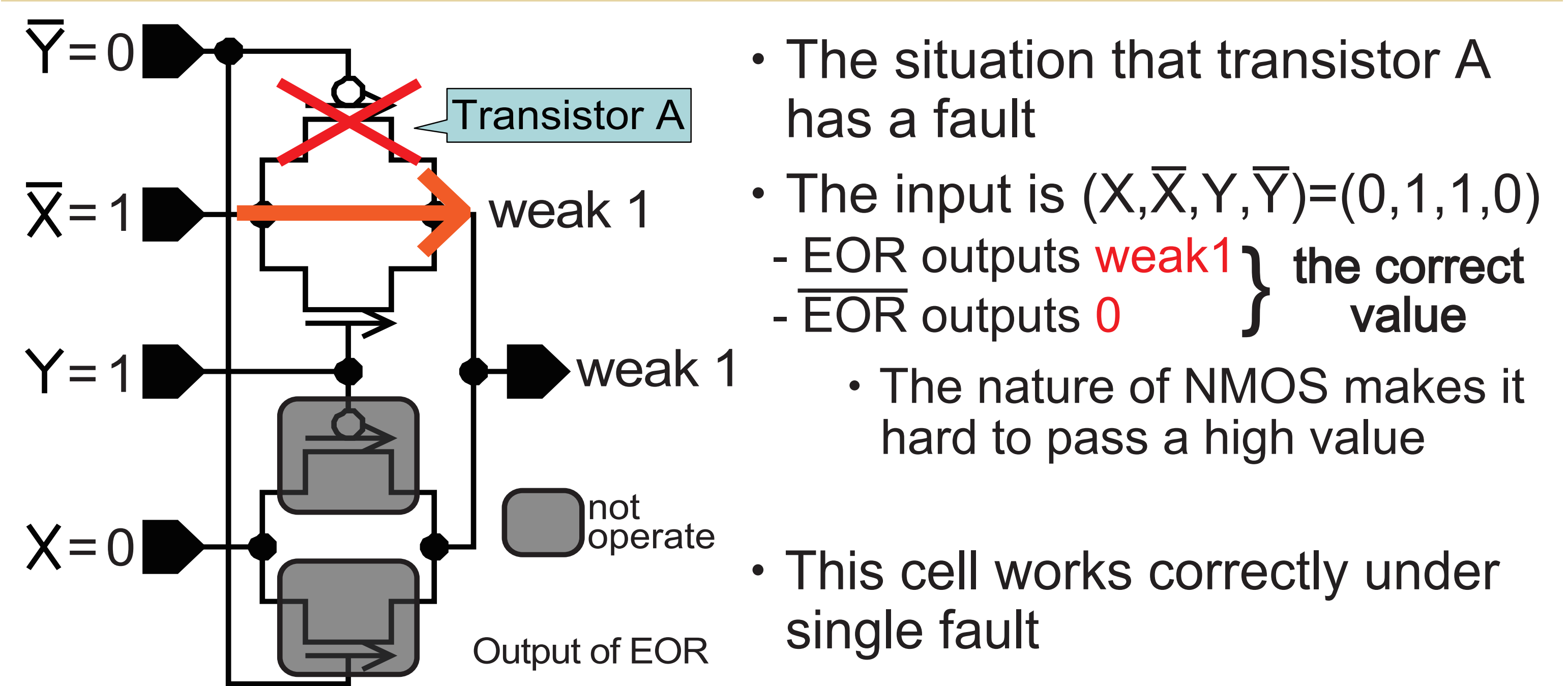
### Basic idea of HRCs

- A positive and negative logic is used in input and output
- Transmission gates are used as base elements
  - The amount of transistors is higher than in traditional cells
  - By using transmission gates, we can arrange transistors evenly

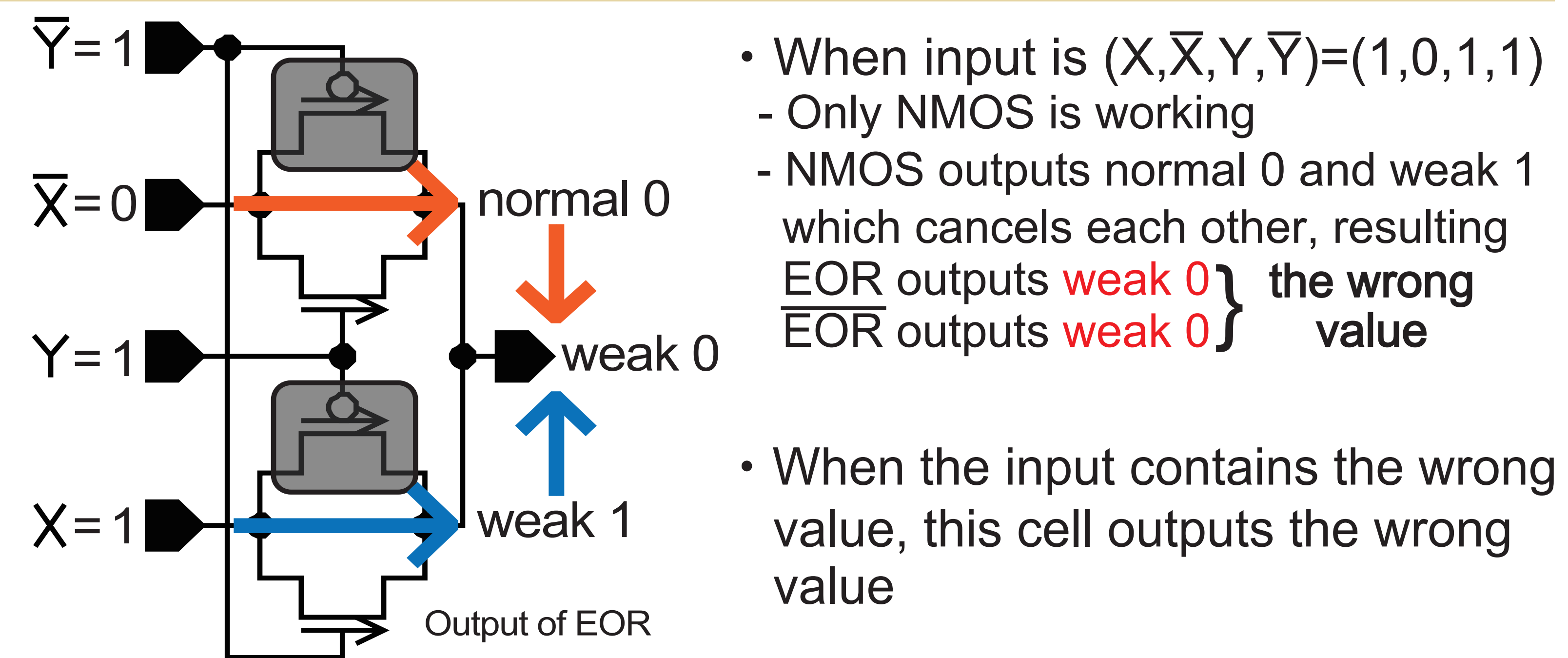


### Behavior of HRCs

#### With single fault

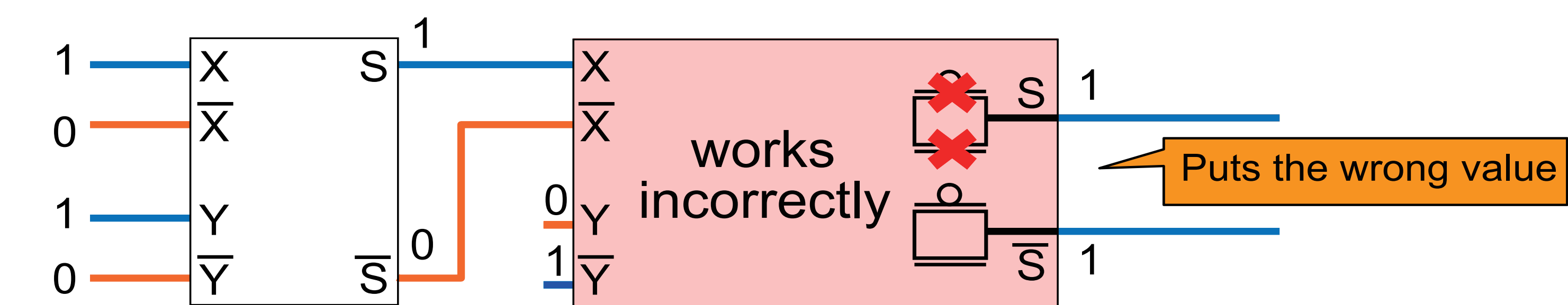


#### With the wrong value

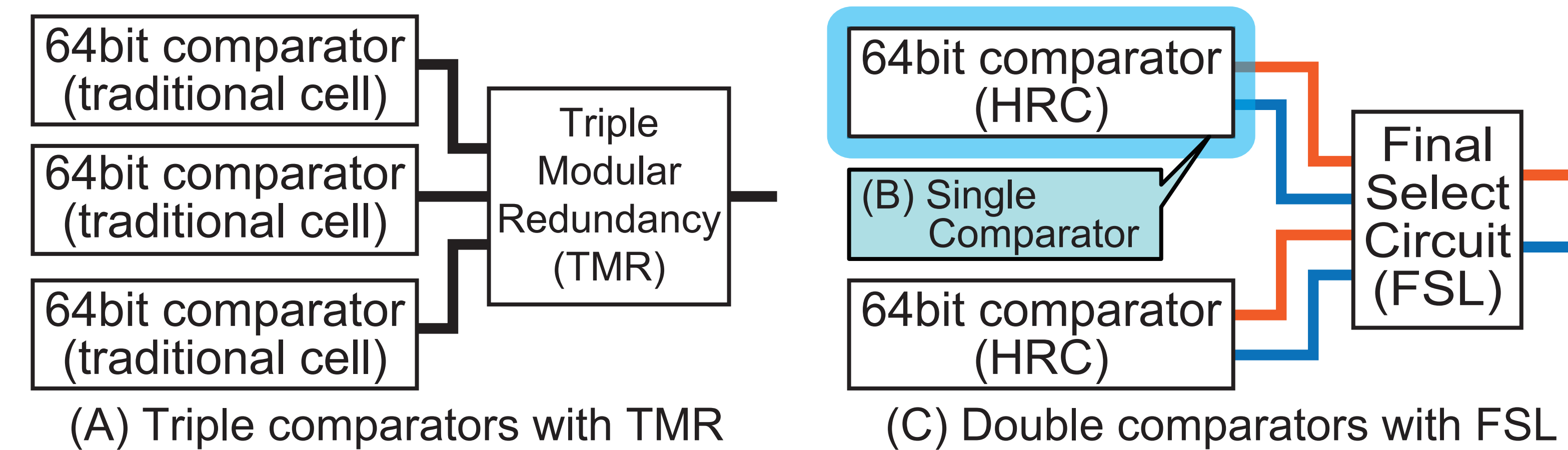


### The correct value and the wrong value

- When either of transistors in transmission gate has a fault
  - An HRC **works correctly** and outputs either (0,1) or (1,0)
  - The output (0,1) or (1,0) are called **the correct value**
- When both of transistors in transmission gate have faults
  - An HRC **work incorrectly** and outputs either (0,0) or (1,1)
  - The output (0,0) or (1,1) are called **the wrong value**



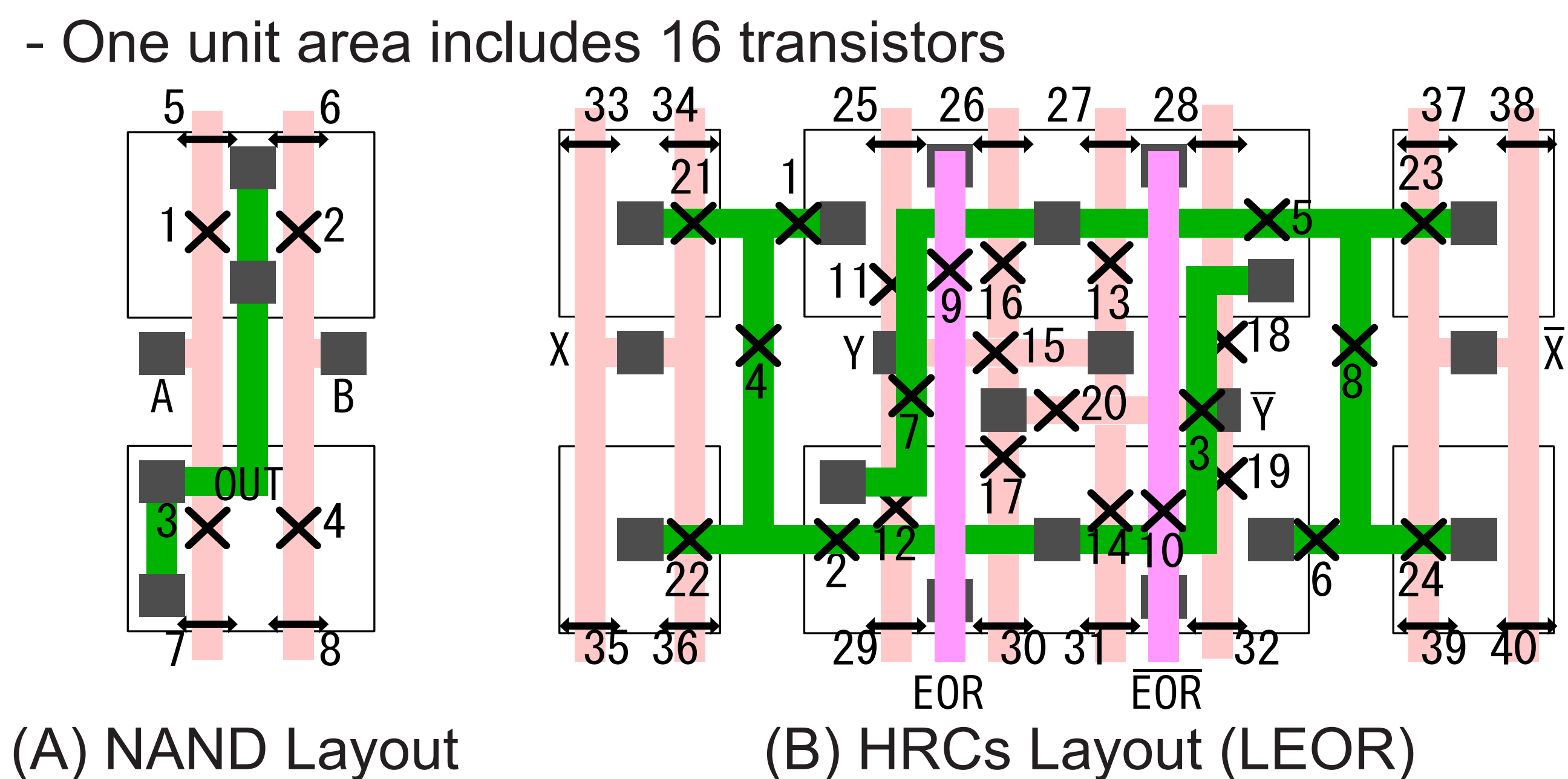
### Implementation of 64bit comparators



- We evaluated three 64bit comparators
  - (A) Triple traditional cell comparators with TMR
  - (B) A single HRC comparator
  - (C) Double HRC comparators with the Final Select Circuit (FSL)

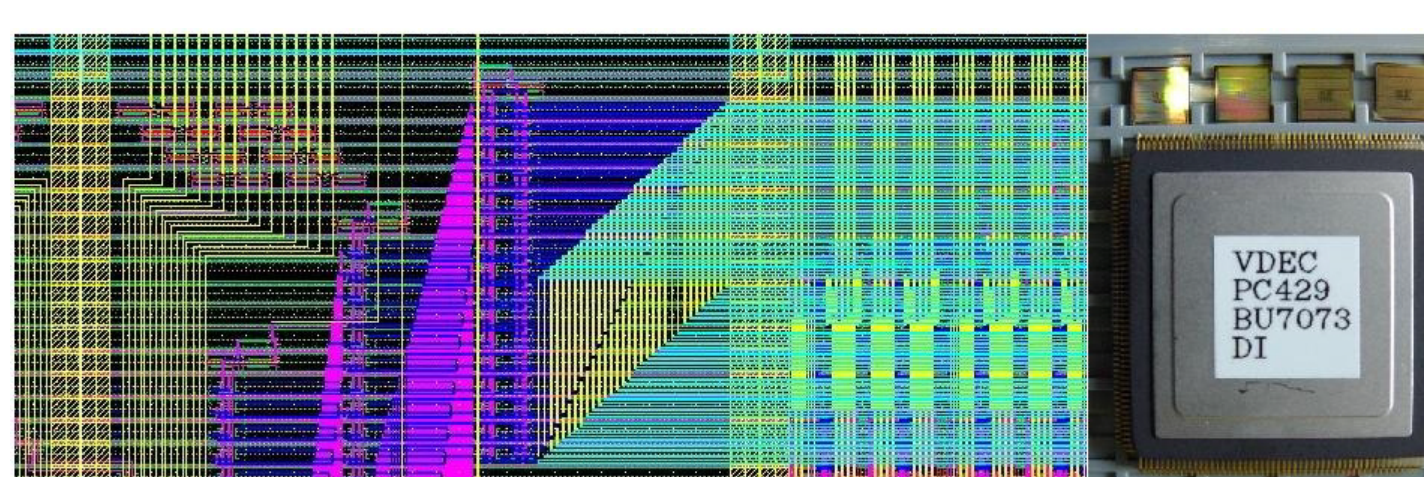
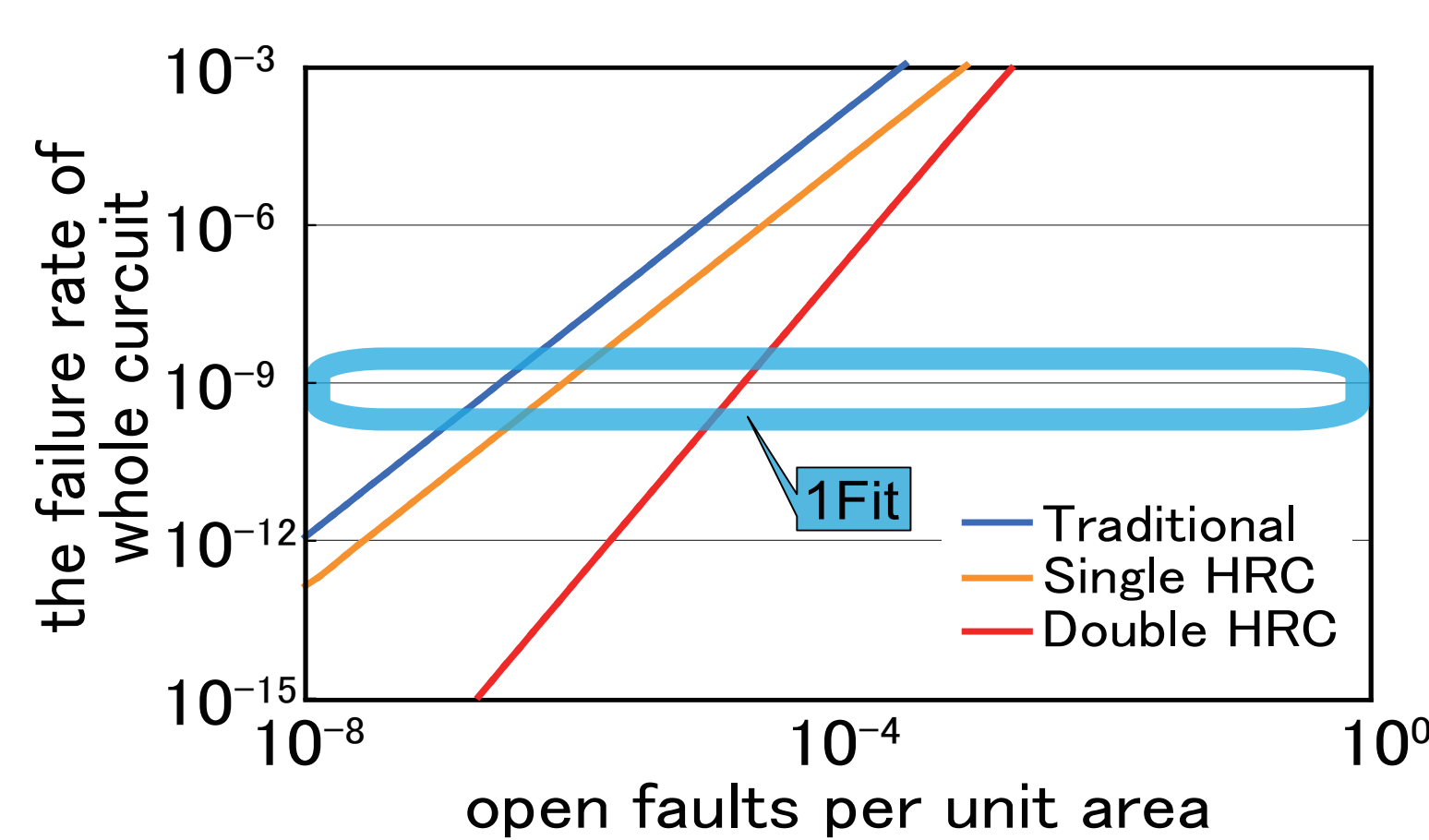
### Proposed new fault model

- **Two types of open faults** are assumed in the proposed fault model
  - One of the lines in the cell has come down (x in Figures)
  - An open fault has assumed between the source and the drain of the MOS ( $\leftrightarrow$  in Figures)
- **The open fault probability per unit area** is used in a calculation of fault tolerance
  - One unit area includes 16 transistors



### Evaluation

Circuit	Area	#Trans.	Delay[ps]
Traditional	432	5364	1063.3
Single HRC	312	5472	923.9
Double HRC	624	11200	1017.7



- The number of transistors in a single HRC is approximately equal to triple traditional cell; however the delay of a single HRC is lower than traditional cell
- On 1Fit, double HRC comparators tolerates **67 times** more open faults per unit area than triple traditional cell comparators
  - $1\text{Fit} = \frac{1 \text{ failure}}{10^9 \text{ hours of operation}}$
- We made a chip which contains a single HRC comparator with single fault and observed that the circuit outputs the wrong value