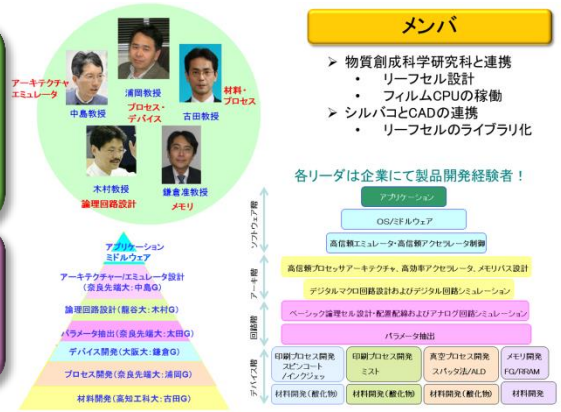
**物資・人・動物等探索・有効利用・配備、インフラの劣化予測・異常検知**
**無数のデバイスが補完し社会全体をカバー**
**電子回路と筐体構造物の物理的融合により製造コスト低減**

**回路作製・安定化 早期応用**

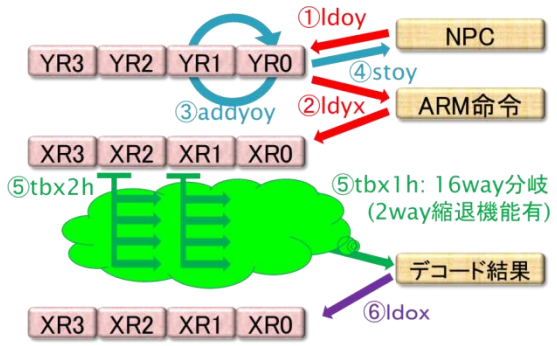
**極めて小さな回路により 実用回路の機能を再現**

**物理的には低品質でも 実環境では相互補完**

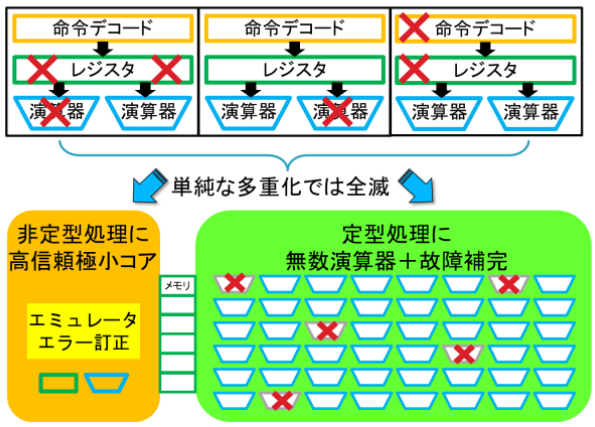



## ゲスト命令デコード機能

➢エミュレータサイズ抑制のため2段階デコード

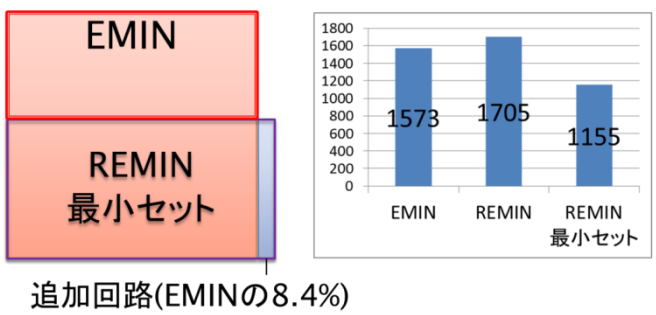



## 背景




## 高信頼化の検討：エラー挿入とレベル2冗長化

## 故障個所をエミュレータが回避して続行




追加回路(EMINの8.4%)

EMINの回路のうち約35%までの故障を許容

## FPGA上でも動作

命令88種,34ピン,Addr/Data 24/8bit

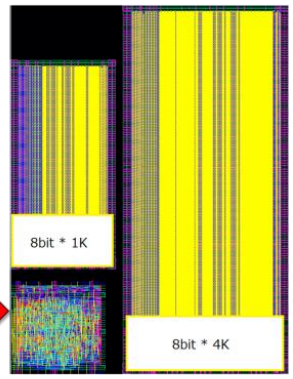
| | |
|---|---|
| in | RST,CLK,C_XINT |
| out | C_XACK |
| out | M_XREQ,M_ADSX,M_WEX,M_BSTMX |
| in | M_XGNT,M_RRDY |
| io[23:0] | M_AD |

## インタフェースを維持しさらに小型化

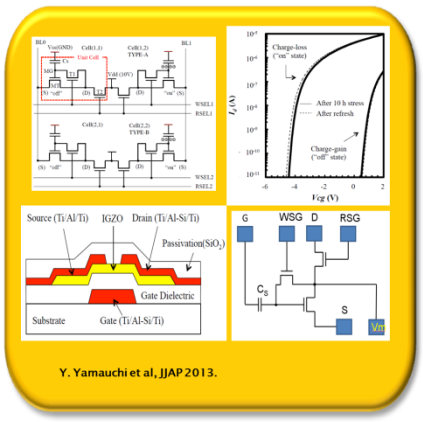
命令88種
PC,LR(12bit),WR,CC
XR3-0,YR3-0
0.18μ…0.24mm角
2in-NAND換算…2643
Tr数…10000

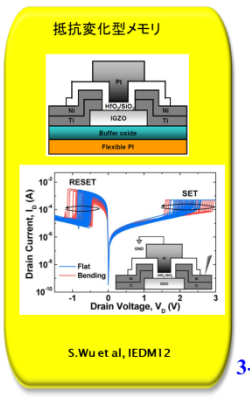
命令55種
PC(10bit),TR3-0,CC
0.18μ…0.20mm角
2in-NAND換算…1748
Tr数…7000(<M6502)

ARM7TDMIは74000



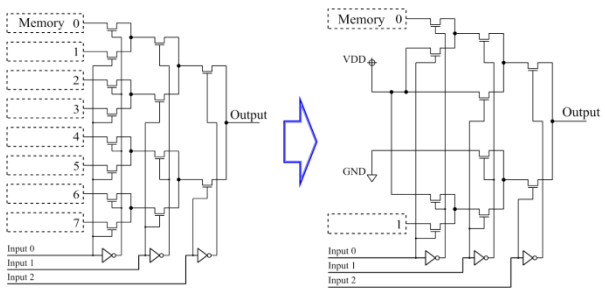

## メモリ素子




## Partially Programmable Circuit

**訂正可能な故障は維持しつつ、**
**LUTで実現可能な論理を限定し，面積を削減する**



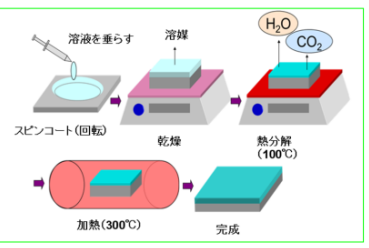

3-input LUT(最適化前)：164 Tr.　3-input LUT(最適化例)：52 Tr.

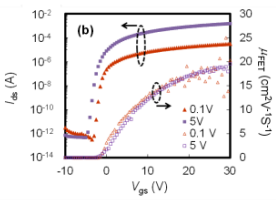
## FreeのAlliance-5.0を使用した場合

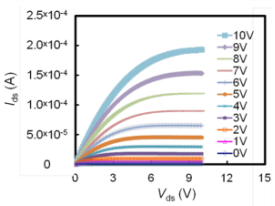
INV,2in-NAND,NOR,XOR,FF
合計4300セル
Tr数…21000
0.35μ5層配線0.78mm角,2層配線0.96mm角
10μインクジェットプリンタ仮定
2層配線で27mm角

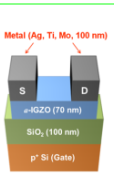
今後、IGZO向けセル開発

## スピンコート法による薄膜トランジスタの作製



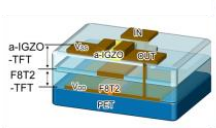



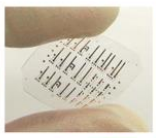



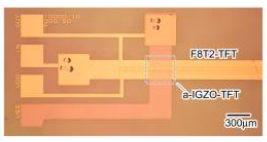




産経新聞 5.12

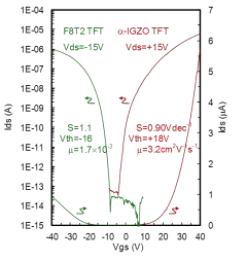
## 酸化物半導体TFTと有機半導体TFTによる積層CTFT回路



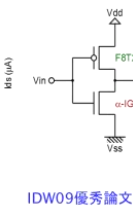



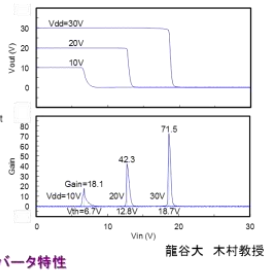



積層CTFT回路




TFT特性



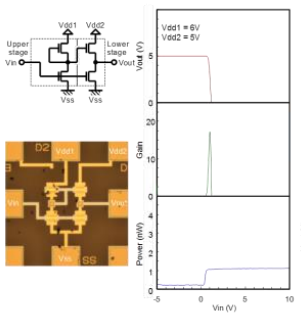

IDW09優秀論文賞受賞

インバータ特性

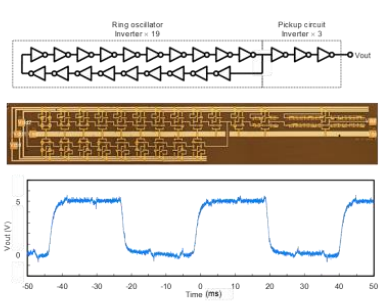
龍谷大 木村教授

## アモルファスIn-Sn-Zn-O TFTによる擬CMOS回路

龍谷大 木村教授




インバータ




リングオシレータ

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